Serial No.: 10/617,638
Filed: July 11, 2003

REMARKS

This Amendment is being filed in response to an Office Action dated January 21, 2004. The fee for a one-month extension of time is being submitted herewith. Reconsideration and allowance of the claims in view of the amendments made above and remarks to follow is respectfully requested.

Specifically, pending claims 12-25 stands rejected as being anticipated by U.S. Patent No. 4,661,806 (Peters). Applicants respectfully traverse this rejection.

Prior to discussing the cited patent in detail, Applicants take this opportunity to point out the patentable features of the present invention, which are now recited in the amended claims. The essence of the patentability of Applicants' invention lies in the novel and unobvious construction of a storage system in combination with the claimed electronic memory device. Applicants respectfully submit that the cited art neither describes or suggests a storage system with an electronic memory device as claimed. Specifically, Applicants respectfully submit that Peters lacks any description or suggestion of a memory device that receives the signals for initiating transmission of the individual code at the ***same*** connections from which the serially transmitted code emanates.

For example, claim 12 now affirmatively recites that the serial transmission of the individualized code is generated between the first and second connections ***and*** that the transmission is initiated by signals across the same two connections. Similarly, claim 13 recites that the serial transmissions originate from the first connection ***and*** are initiated by signals on the same connection. Likewise, claim 14 recites a logic circuit for signaling the data connection of the selected electronic memory device ***and*** transmission of the code emanating from the same data connection. Similar amendments have been made in the remaining independent claims (i.e. claim 15: " ... a serially transmittable individualized code *triggerable **and** receivable* from the two terminals"; claim 16: signaling of a memory device via its data and ground connections ***and*** receiving an individualized code originating from the data and ground connections..."; claim 17: "signaling of a memory devic via its data and ground connections to transmit its individualized code ***and***

receiving the code from the signaled data connection; and claim 18: "addressing logic to initiate transmissions from the two terminals and a processor to receive a transmitted individualized code from the ***same*** two terminals"). Applicants respectfully submit that Peters not only lacks a description of a storage system that could use a memory device as claimed, but actually requires a memory device with a patentably different configuration.

That is, although Peters describes a means for storage and controlled access to a large number of keys, the embodiment that comprises an embedded electronic circuit to provide keyholder identification data is patentably different from that which is claimed by Applicants. As described in Peters in col. 8, line 38 to col. 9, line 47 (see also Figs. 10-12), the address decoding circuits select one of the EEPROMs and the interface to the selected EEPROM, among other things, ***must provide a clock signal on line 306 for providing data input on line 312 and data output on line 308***. Along with the source and drain voltages being provided to the source and drain lines (314) and the need for a chip select line (CS), it can be seen that Peters requires more than two electrical connections and, specifically, lacks any description or suggestion of providing multiple functions through common connections.

Applicants respectfully submit this distinction is important. That is, Applicants respectfully submits to being the first to be able to use a two connection electronic memory device in a storage system as claimed. The disclosure of the preferred Dallas DS1990, along with the figures and what one skilled in the art easily understands, in which both the signaling (e.g. the clock signals) to the memory device and the data output (e.g. the transmittable code) from the memory device occurs at the same two connections, is a configuration neither described nor suggested by Peters.

Because Peters ***requires*** a six (6) pin chip, and more importantly, requires separate pins to receive the clock signals and output data, Applicants respectfully submit that the invention as now claimed is patentable over the Peters disclosure. Moreover, because Applicants believe they are the first in time to use a two terminal device in the claimed manner, Applicants respectfully submit the claims are now in condition for allowance, and notice to the effect that pending claims 12-25 are in condition for allowance is earnestly solicited.

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Applicants have made a sincere and diligent effort to place this application in condition for allowance. However, if any issues remain, it is respectfully requested that the undersigned be contacted prior to the issuance of another office action.

Respectfully submitted,

By: _____

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